

WHAT IS CLAIMED IS:

1 1. A digital line build out circuit comprising:
2 a memory storing a plurality of digitized waveforms;
3 a selection circuit, coupled to said memory, to select certain ones of said
4 waveforms corresponding to an anticipated amount of signal degradation over a transmission
5 line; and
6 a digital to analog converter to convert said certain ones of said waveforms
7 into analog waveforms for transmission.

1 2. The circuit of claim 1 further comprising:
2 a counter having an output coupled to inputs of said memory for sequentially
3 selecting multiple samples of said digitized waveforms during a period.

1 3. The circuit of claim 1 wherein said memory comprises a ROM.

1 4. The circuit of claim 1 further comprising:
2 a combining circuit, coupled between said memory and said digital to analog
3 converter, to combine a portion of a current digitized waveform with a portion of at least one
4 previous digitized waveform.

1 5. The circuit of claim 4 wherein said combining circuit includes at least one
2 delay element for delaying an output of said memory for said previous digitized waveform
3 for combination with said current digitized waveform.

1 6. The circuit of claim 5 wherein said delay element delays a data bit, and
2 further comprising a circuit for gating a portion of said digitized waveform from said memory
3 based on a value of said data bit.

1 7. The circuit of claim 4 wherein said combining circuit combines portion of a
2 current waveform with portions of three previous waveforms.

1 8. A digital line build out circuit comprising:
2 a memory storing a plurality of digitized waveforms;
3 a selection circuit, coupled to said memory, to select certain ones of said
4 waveforms corresponding to an anticipated amount of signal degradation over a transmission
5 line;

6 a digital to analog converter to convert said certain ones of said waveforms
7 into analog waveforms for transmission;
8 a counter having an output coupled to inputs of said memory for sequentially
9 selecting multiple samples of said digitized waveforms during a period; and
10 a combining circuit, coupled between said memory and said digital to analog
11 converter, to combine a portion of a current digitized waveform with a portion of at least one
12 previous digitized waveform.

1 9. A digital line build out circuit comprising:
2 a memory storing a plurality of digitized waveforms corresponding to different
3 anticipated amounts of signal degradation over a transmission line, each of said digitized
4 waveforms having a plurality of separately addressable portions;
5 a data line coupled to a plurality of serial delay elements;
6 a plurality of gating circuits having a first input coupled to one of said data
7 line and an output of each of said delay elements, and a second input coupled to an output of
8 said memory for one of said separately addressable portions;
9 a combining circuit having inputs coupled to outputs of said gating circuits for
10 combining multiple ones of said separately addressable portions;
11 a digital to analog converter coupled to an output of said combining circuit;
12 a configuration input, coupled to said memory, for selecting a desired one of
13 said plurality of digitized waveforms; and
14 a counter, coupled to said memory, for sequentially selecting a plurality of
15 digitized values for said separately addressable portions.

1 10. The circuit of claim 9 wherein said memory is a ROM.

1 11. The circuit of claim 9 wherein said memory comprises a plurality of
2 memories.

1 12. The circuit of claim 9 where said gating circuits comprise a multiplier
2 circuits.

1 13. The circuit of claim 9 wherein said gating circuits comprise selector
2 circuits.